

174/297

IN THE STATES PATENT AND TRADEMARK OFFICE

Applicants : San Wong et al.

Application No. : 10/725,898

Confirmation No. : 3367

Filed : December 1, 2003

FOR : BIT ERROR RATE TESTER IMPLEMENTED

IN A PROGRAMMABLE LOGIC DEVICE

Art Unit : 2133

New York, New York 10020

December 21, 2005

Mail Stop AMENDMENT Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450

TRANSMITTAL LETTER FOR INFORMATION DISCLOSURE STATEMENT

Sir:

Transmitted herewith is an Information

Disclosure Statement in the above-identified application.

This Statement is submitted:

- [] within three months of the application filing date;
- [X] more than three months from the application filing date but before the mailing date of the first Office Action on the merits.

In accordance with 37 C.F.R. § 1.97, submission of this Statement requires no fee. However, if for any reason a fee is due, the Director is hereby authorized to charge payment of any fees required in connection with

this Information Disclosure Statement to Deposit Account No. 06-1075, Order No. 000174.0297. A duplicate copy of this letter is transmitted herewith.

Respectfully submitted,

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| INFORMATION | DISCLOSURE |
|--------------------|-------------------|
| STATEMENT B | Y APPLICANT |

Applicant Number 10/725,898

Filing Date December 1, 2003

First Named Inventor San Wong

Art Unit 2133

Examiner Name Not Yet Assigned

Attorney Docket Number 174/297

Confirmation Number 3367

(Use as many sheets as necessary)

Sheet 1 of 1

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|---------------------------------|--------------------------|--|----------------|--|
| NON PATENT LITERATURE DOCUMENTS | | | | |
| Examiner Initials* | Cite No. ¹ | | T ² | |
| | | "Jitter Fundamentals: Agilent N4900 Serial BERT Series Jitter Injection and Analysis Capabilities," Application Note, Agilent Technologies, November 2003, pp. 1-24. | , I, | |
| | | "Understanding and Characterizing Timing Jitter," Tektronix, www.tektronix.com/jitter, 2003, pp. 1-24. | | |
| | | "Annex 48B: Jitter test methods," IEEE Std 802.3ae-2002,IEEE, 2002, pp. 505-514. | | |
| | | Wang, et al., "Equalization Techniques," Carleton University, presentation slides. | | |

| Examiner | Date |
|-----------|------------|
| Signature | Considered |

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.